Presentation outline

- **Requirements**
  - Basic requirements
- **Implementation**
  - Use PCI acquisition hardware on PC platform
- **PCI acquisition hardware details**
  - Overview, basic capabilities
  - Secondary capabilities
  - Selected design details
- **Platform details**
  - Choice of hardware
    - Choice for HW development systems
  - Choice of software
    - Choice for SW development components
  - Current Status

BPM Data Acquisition Electronics

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Data acquisition platform requirements

- **Capable of acquiring 60hz pulsed beam**
- **Simultaneous acquisition on multiple channels**
  - 8 channels for phase/position
- **1 ms pulse length**
- **At least 40Mhz sample rate**
  - 40/20Mhz for phase/position measurement
- **No known real time requirements**

Design Overview

- Develop basic acquisition front end
- Utilize standard bus to move data to commercial motherboard
- Perform necessary calculations on system CPU using high level software
- Entire unit becomes stand alone instrument with ethernet (EPICS channel access) interface to outside world

Design details

- **Use PCI as standard interface bus**
  - Choice of form factors (standard, compact, PMC)
  - Bridging between form factors easily accommodated
  - Excellent 3rd party hardware support
  - High performance (easily achieves >100Mb/s)
- **PC as instrument CPU**
  - Inexpensive, standard design
  - Good performance
  - Unmatched choice of software
  - Industrial, high reliability, and embedded variants available from many vendors

PCI acquisition hardware details

- **40Mhz bandwidth from AFE on 8 channels**
  - Capable of 80mhz on 8 channels
- **1mS buffer depth**
  - 40K samples at 40MHz
- **Sample memory implemented in 16 bit FIFOs**
  - Depths up to 256K available now
- **DMA upload to host memory**
  - Unloads main CPU from I/O bus bottleneck
- **Acquisition timing capability**
  - 10 internal timing channels provide acquisition gates
  - Multiple events per channel supported

Secondary hardware functions

- **Single Industry pack site**
  - Connects to timing triggers and AFE daughter card
  - 50 pin external connection
  - Intended for SNS timing decoder
  - 8MHz IP standard, all standard functions supported
- **Low speed utility bus**
  - Connects to AFE
  - Used to configure AFE functions

Design details

- **Implemented on standard PCI form factor**
- **Digital logic implemented in single FPGA**
  - Bus mastering PCI interface built in by vendor
  - Generous timing and utilization margins at this time
- **Programmable sequencers**
  - Execute simple programs to implement functions
  - Acquisition timing
  - DMA
  - IP and utility bus
  - Sequencer functionality can be changed on the fly
- **Two clock synthesizers**
  - Quartz stabilized fixed acquisition clock
  - Programmable digital acquisition clock
  - Allows direct decimation during acquisition

Link Interface

- **SNS Links**
  - Two custom (SNS-specific) links
    - **Event Link:** carrier locked to 16 x revolution frequency,
    - **Real Time Data Link (RTDL):** Several 24 bit frames broadcast before each pulse
  - Broadcast over fiber star, sourced by generators in the sequencer system
- **Embedded receiver**
  - Industry Pack
    - **Inputs:** RTDL on copper and event link on copper, both transformer isolated; misc. TTL compatible inputs, function programmable within gate array
    - **Outputs:** low jitter (10s of ps) clock at 64 times the ring revolution frequency (not used in RF BPM/phase application), transformer isolated; several 3.3 V pulse outputs; misc. programmable outputs
    - **Registers:** RTDL frames (timestamp, link period, beam mode, etc…) updated before each macropulse; event list updated on each macropulse; pulse control registers (source, delay, width)
  - In RF BPM/phase application:
    - the pack resides on the PCI card; inputs/outputs are all routed to daughtercard
    - One pulse output provides a gate to mark expected time of beam data
    - After each pulse, data from registers is moved to PC memory along with digitizer data. LabVIEW application can then process data based on event/mode and timestamp the results

PC hardware issues

- **Performance**
  - Standard motherboards offer best price/performance
  - Passive backplane designs offer ease of maintenance
  - Embedded units offer robust packaging and low power
  - Compact PCI offers a standard robust package for high price
- **Reliability**
  - Standard edge connectors have limited insertion life
  - Requirement for disk storage for some software solutions
  - Typical use of cheap power supplies in some form factors
- **Form factor**
  - Rack mount
  - Desk top
  - Compact PCI

Desired PC configuration

- **Standard motherboard**
  - Readily available
  - Best performance
- **Standard edge connectors**
  - Compatibility with vast selection of commercial hardware
  - Experience during development will help better quantify insertion life risk
- **Solid state disk**
  - PC type II (ATA) FLASH
- **Rack mount form factor**
  - Server chassis designed for industrial environments
  - Desktops can be used for most development

Embedded Software

- **National Instruments Labview for application development**
  - Large selection of compatible hardware from many vendors
  - Already in use for many years by diagnostics team
  - Superior tools for analysis and display
- **Embedded Windows NT/2000 operating system**
  - Embedded toolkit allows custom versions to be generated, which only include desired functions
  - Extended functions allow for automatic login, running from read only media, remote administration, and message handling
  - Supports all hardware usable in regular NT/2000 systems
  - Real time extension available to handle acquisition and time stamping functions

Current status

- **PCI data acquisition board**
  - PC board completed
  - FPGA simulations finished with the exception of DMA controller
- **Test build of operating system completed**
  - Supports Labview development and run time
  - Supports operation from read only media
  - Allows remote administration
- **Interface to real time subsystem prototyped**
  - Mimics interface to DMA buffers, periodic acquisition, and time stamp generation
  - Initializes data from disk files
  - Labview interface completed and in use
  - Allows significant software development on any PC